What is Claimed is:

1. A digital control logic circuit having a characteristic of time hysteresis for controlling transition of a digital control signal during a predetermined period, comprising:

a first time hysteresis unit having a characteristic of time hysteresis when an input signal transits from a first level to a second level; and

a second time hysteresis unit connected in series to the first time hysteresis unit having a characteristic of time hysteresis when the input signal transits from the second level to the first level.

2. The circuit according to claim 1, further comprising an inverter for inverting an output signal from said second time hysteresis unit.

3. The circuit according to claim 1, wherein the first time hysteresis unit comprises:

a latch unit for maintaining an output signal at a predetermined level;

an inverter for inverting the output signal from the latch unit; and

a first delay unit connected to the latch unit in a feedback structure, which delays an output signal from the inverter for predetermined time of a first delay.

4. The circuit according to claim 1, wherein the second time hysteresis unit comprises:

a latch unit maintaining an output signal at a predetermined level;

an inverter for inverting the output signal from the latch unit; and

a second delay unit connected to the latch unit in a feedback structure, which delays an output signal from the inverter for predetermined time of a second delay.

5. The circuit according to claims 3 or 4, wherein the second delay time is more than two times longer than the first delay time.

6. A digital control logic circuit having a characteristic of time hysteresis, comprising:

a delay unit for delaying an input signal; and

a state machine for receiving the input signal and an output signal from the delay unit, having an output value determined under control of the transition state, and

adjusting its state according to the output value to have a characteristic of time hysteresis for both cases when the input signal transits from low level to high level and when the input signal transits from high level to low level.

7. The circuit according to claim 6, wherein the state machine is a 2bit state machine.